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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,974	09/29/2000	STAN W BOWLIN	F-316	1735

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DELLETT AND WALTERS
310 S.W. FOURTH AVENUE
SUITE 1101
PORTLAND, OR 97204

EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/675,974	Applicant(s) BOWLIN, STAN W
	Examiner Christopher E. Lee	Art Unit 2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Preliminary Amendment filed on 29th of September, 2000. No claims has been amended; no claims has been canceled; and no claims has been newly added. Currently, claims 1-9 are pending in this application.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Masterson et al. [US 5,073,851; hereinafter Masterson].

Referring to claim 1, AAPA discloses a method for transferring data on a bus (See page 2, line 34 through page 3, line 4) from a source (i.e., MAC) to at least two destinations (i.e., DSP and SDRAM), comprising the steps of: supplying data from said source (i.e., MAC) to first of said at least two destinations (i.e., DSP) as a read data operation (See page 2, line 35); and supplying data to a second of said at least two destinations (i.e., SDRAM) as a write operation (See page 3, line 2).

AAPA does not teach said data transferring (i.e., read operation and write operation on said data) would been substantially simultaneously operated.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a read operation of a data from a source (i.e., main memory 15 of Fig. 2) to a first destination (i.e., CPU 12 of Fig. 2) is substantially simultaneously (See claim 1 and col. 5, lines 57-60) overlapped with a write operation of said data from said source to a second destination (i.e., cache 18 of Fig. 2) under being controlled by a timing controller (i.e., gate array 34 of Fig. 2). Refer to col. 5, lines 37-68.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of data transferring control (i.e., by the timing controller in gate array), as disclosed by Masterson, in said method of data transferring, as disclosed by AAPA, so as to pass said data to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation). Refer to Masterson, col. 3, lines 60-65.

Referring to claim 4, AAPA teaches that at least one of said at least two destinations (i.e., SDRAM and DSP) comprise addressed data devices (i.e., SDRAM is a synchronous dynamic random access memory, which is accessed through an address bus, and DSP is a digital signal processor, which is accessing an external data through said address bus, too).

Referring to claim 5, AAPA teaches said at least one destinations comprises a microprocessor (i.e., DSP stands for Digital Signal Processor).

Referring to claims 6 and 7, AAPA teaches said at least one destinations comprises a memory storage, which is SDRAM (i.e., SDRAM stands for Synchronous Dynamic Random Access Memory).

Referring to claim 8, AAPA discloses an apparatus (i.e., network test device) for transferring received data from a network (See page 2, line 34 through page 3, line 4), comprising: a bus (See page 3,

line 1); a media access controller (i.e., MAC in page 2, line 35) for putting said received data from said network onto said bus (See page 2, lines 34-35); a microprocessor (i.e., DSP) for reading said data from said bus (See page 2, line 35); a memory (i.e., SDRAM) for writing said data from said bus into said memory (See page 3, line 2).

AAPA does not disclose a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write said data to said bus, said memory write said data to said memory and said microprocessor read said data substantially simultaneously.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a timing controller (i.e., gate array 34 of Fig. 2) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) a media access controller (i.e., main memory 15 of Fig. 2), a microprocessor (CPU 12 of Fig. 2) and a memory (i.e., cache 18 of Fig. 2) to have said media access controller (i.e., main memory) write said data to said bus (See col. 5, lines 45-54; i.e., wherein in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said media access controller (i.e., main memory) write data to said bus), said memory (i.e., cache) write said data to said memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said microprocessor (i.e., CPU) read said data (i.e., read access of the main memory, furnished by CPU; See col. 5, lines 58-59) substantially simultaneously (See col. 5, lines 37-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said timing controller, as disclosed by Masterson, in said apparatus, as disclosed by AAPA, so as to pass said data to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage

of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation). Refer to Masterson, col. 3, lines 60-65.

5. Claims 2, 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Masterson [US 5,073,851] as applied to claims 1 and 4-8 above, and further in view of DeSouza et al. [US 5,379,289 A; hereinafter DeSouza].

Referring to claim 2, AAPA, as modified by Masterson, discloses all the limitations of the claim 2 except that does not teach said source comprises a non-addressed data device.

DeSouza discloses a source (i.e., media access controller in Fig. 6) comprises a non-addressed data device (i.e., receiver FIFO 20 of Fig. 6; See col. 2, lines 5-14, wherein in fact that the data stored in the receiver FIFO is then transferred to a user system implies that said source (i.e., media access controller) comprises a receiver FIFO, which is a non-addressed data device since said stored data is transferred to said user system without being accessed by said user system).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said receiver FIFO, as disclosed by DeSouza, in said source (i.e., MCA), as disclosed by AAPA, as modified by Masterson, so as to transfer incoming data stream to said destinations (e.g., memory and processor) in succession (i.e., first-in-first-out sequence) with the advantage of providing a buffering function, which is well known to one of ordinary skill in the art of digital circuit design.

Referring to claim 3, DeSouza teaches said source comprises a FIFO device (i.e., receiver FIFO 20 of Fig. 6).

Referring to claim 9, AAPA discloses an apparatus (i.e., network test device) for transferring data (See page 2, line 34 through page 3, line 4), comprising: a bus (See page 3, line 1); a data source (i.e., MAC in page 2, line 35) connected to said bus for putting data onto said bus (See page 2, lines 34-35); a microprocessor (i.e., DSP) connected to said bus for reading said data from said bus (See page 2, line 35);

a memory (i.e., SDRAM) connected to said bus for writing said data from said bus into said memory (See page 3, line 2).

AAPA does not disclose a timing controller connected to said data source, said microprocessor and said memory for controlling said data source, said microprocessor and said memory to have said data source put said data onto said bus, said memory write said data to said memory and said microprocessor read said data substantially simultaneously.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a timing controller (i.e., gate array 34 of Fig. 2) connected to a data source (i.e., the gate array 34 is connected to the main memory 15 via the main memory control line and the main memory address line, shown in Fig. 2), a microprocessor (i.e., the gate array 34 is connected to the CPU 12 via the control lines, shown in Fig. 2) and a memory (i.e., the gate array 34 is connected to the cache 18 via the cache memory control line and the cache address line, shown in Fig. 2) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) said data source (i.e., main memory 15 of Fig. 2), said microprocessor (i.e., CPU 12 of Fig. 2) and said memory (i.e., cache 18 of Fig. 2) to have said data source (i.e., main memory) put said data onto said bus (See col. 5, lines 45-54; i.e., wherein in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said data source (i.e., main memory) put data to said bus), said memory (i.e., cache) write said data to said memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said microprocessor (i.e., CPU) read said data (i.e., read access of the main memory, furnished by CPU; See col. 5, lines 58-59) substantially simultaneously (See col. 5, lines 37-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said timing controller, as disclosed by Masterson, in said apparatus, as disclosed by AAPA, so as to pass said data to said one of at least two destinations as a read operation, and to said

other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation). Refer to Masterson, col. 3, lines 60-65.

AAPA, as modified by Masterson, does not expressly teach said data source is a FIFO data source.

DeSouza discloses a data source (i.e., media access controller in Fig. 6) comprises a FIFO data source (i.e., receiver FIFO 20 of Fig. 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said receiver FIFO, as disclosed by DeSouza, in said data source (i.e., MCA), as disclosed by AAPA, as modified by Masterson, so as to transfer incoming data stream to said destinations (e.g., memory and processor) in succession (i.e., first-in-first-out sequence) with the advantage of providing a buffering function, which is well known to one of ordinary skill in the art of digital circuit design.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Regarding to the incoming data processing system,

Raab et al. [US 6,219,928 B1] disclose serial network for coordinate measurement apparatus.

Regarding to the communication access control,

Fallside et al. [US 6,326,806 B1] disclose FPGA-based communications access point and system for reconfiguration.

Gulick [US 6,326,806 B1] discloses subordinate bridge structure for a point-to-point computer interconnection bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

CEL/ CEL
February 6, 2003

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100